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9-20-02

PATENT
Attorney Docket No.: AHA-02201

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Eric John Hewitt et al.

Serial No.: 09/826,443

Filed: April 4, 2001

For: **ENHANCED TURBO PRODUCT
CODE DECODER SYSTEM**

Assistant Commissioner for Patents
Washington, D.C. 20231

) Art Unit: 2819

) Examiner:

) **TRANSMITTAL LETTER**

) 162 N. Wolfe Road
) Sunnyvale, CA 90486
) (408) 530-9700

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Sir:

Enclosed please find a Supplemental Information Disclosure Statement, Form PTO-1449, copies of the references contained thereon, for filing in the U.S. Patent and Trademark Office.

The Commissioner is hereby authorized to charge any additional fee or credit overpayment to our Deposit Account No. 08-1275. **An originally executed duplicate of this transmittal is enclosed for this purpose.**

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: September 9, 2002

By: Jonathan O. Owens
Jonathan O. Owens
Reg. No.: 37,902

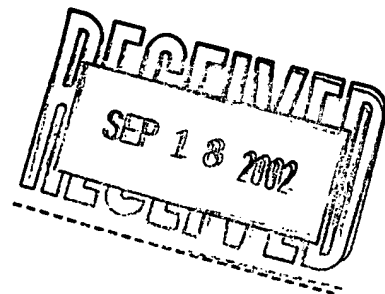
Attorneys for Applicants

CERTIFICATE OF MAILING (37 CFR § 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington D.C. 20231

HAVERSTOCK & OWENS LLP.

Date: 9/9/02 By: [Signature]





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) Examiner:

) **SUPPLEMENTAL INFORMATION**
) **DISCLOSURE STATEMENT**

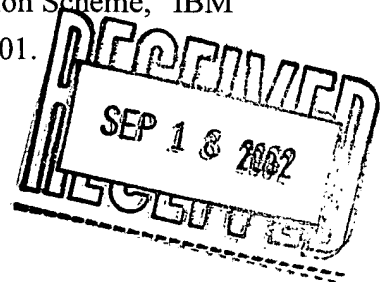
) 162 N. Wolfe Road
) Sunnyvale, CA 94086
) (408) 530-9700

Sir:

The citations listed below, a copy attached, may be material to the examination of the above-identified application, and are therefore submitted in compliance with the duty of disclosure defined in 37 C.F.R. §§ 1.56 and 1.97. The Examiner is requested to make these citations of official record in this application.

Applicants have become aware of the following printed publications which may be material to the examination of this application:

- U.S. Patent 5,541,955;
- U.S. Patent 6,104,758;
- "Diagnosing On-Card Error Checking and Correcting Operations Using Latched Syndrome Data, IBM Technical Disclosure Bulletin, October 1989, No. NA891026; and
- "Single-Bit Correct, Double-Bit Error Checking/Correction Scheme," IBM Technical Disclosure Bulletin, May 1994, No. NN9405101.



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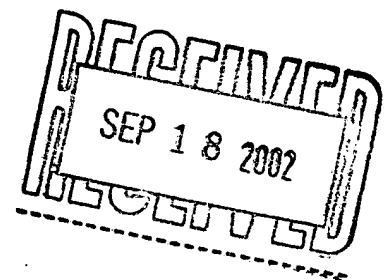
This Supplemental Information Disclosure Statement under 37 C.F.R. §§ 1.56 and 1.97 is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that anyone or more of these citations constitutes prior art.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: September 9, 2002

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Attorneys for Applicants



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